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DESIGN OF HIGH SPEED SUBTHRESHOLD INTERCONNECTS USING MCML TECHNIQUE

Amruta S.Thorat*, R. S. Khule, Dr. S. D.Pable
Department of Electronics and telecommunication, Matoshri College of Engineering & Research centre, India

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ABSTRACT

The recent trend in the VLSI industry toward miniature designs, low power consumption, and increased growth of portable applications compels researchers to design circuit having high speed. This is achieved by operating circuits under subthreshold condition and by designing interconnects using various techniques. This paper presents designing of Subthreshold interconnects using MCML technique which exhibits a decrease in delay in terms of designing of interconnects under subthreshold region as compared to CMOS techniques. Circuit is implemented in 32nm MOS technology using HSPICE. The results illustrates that total delay improvement is achieved by using proposed system which helps the circuit to operate at high speed and it also improves propogation delay and energy delay.

KEYWORDS: MOS current mode logic(MCML), Subthreshold, Delay, Power Delay Product(PDP), Energy Delay Product(EDP), Total delay(Tpd)

INTRODUCTION

Due to scaling of technology to integration level, interconnect resource becomes increasingly valuable in a VLSI chip. The designing of interconnects becomes challenging task due high speed and increased integration of analog circuits with digital blocks. The previously negligible effects of interconnects has been highlighted by quest for high-speed applications. MCML circuits are the preferred logic style as it allows improving the speed, the power efficiency and reducing the switching noise, which are key aspects in VLSI circuits. In these high-speed circuits, the performance degradation associated with the heavily loaded nodes is usually counter acted by inserting drivers. *What is High-Speed?* between its end points the time taken by the signal to travel which cannot be neglected is "High-speed interconnect". The physical extent of the interconnect, the longer the interconnect, the more time required is an obvious factor and influences this definition. Due to their better performance, CML circuits are the best choice for high-speed applications.

The sub-threshold region or weak inversion operation which uses leakage current is regarded as the most power-efficient region of operation for a logic device. This is the region for ultra-low power applications. Conventional CMOS static logic design is popular because of its convenient availability in standard library cells, small area usage, low power dissipation, and high noise margin. But, when operated in sub-threshold region, the static CMOS devices exhibit drastically increasing delays with scaling of supply voltage. This lower speed has been unattractive for many applications till recently. Another problem with static CMOS circuits is that the sub-threshold current is very sensitive. Hence a new technology called MOS current mode logic (MCML) has been evolved. It is a popular logic style for high-speed circuits and robustness. This type of logic was first implemented in bipolar technology and extended for application with MOS transistors.

INTERCONNECTS

Interconnects are used to connect components on a VLSI chip, to connect chips on a multichip module, to connect multichip modules on a system board. In conventional copper interconnects CMOS buffer is used as a buffer or inverter. Interconnect load are represented by RLC lumped model. R, L and C parameters are determines from the

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physical specifications of interconnects. In long interconnects repeaters are inserted to reduce the overall interconnect delay.

Types of interconnects

Interconnects are often classified using the International packaging level hierarchy, which is based on the type of interconnected components and their typical interconnection distances.

On a modern IC chip interconnects can also be broadly characterized into three groups according to the functions they perform.

These are as following:

[1] Signalling interconnects
[2] The clock distribution interconnects
[3] Power and ground supply distribution interconnects

According to the range of their lengths and their cross section dimensions, interconnects can be further subdivided into following three categories.

These are:

[4] Local interconnects
[5] Semi-global or intermediate interconnects
[6] Global interconnects

For long distance communication the global interconnects are used on a chip and have a larger cross sectional area to minimize the resistance. Whereas, the local interconnects have the shortest range and the least cross sectional dimensions. Modern ICs have multiple levels of interconnects to accommodate their large numbers, starting from the local at the lowest level to the global at the top most levels.

Interconnects Overview:

The propagation delay of an *RC* Cu line driven by CMOS driver can be expressed as follows [7]:

$$Id = Rdriv(Cdriv + Cload) + 0.4Rw.Cwl^2 + (Rdriv.Cw + Rw.Cload)l \quad \ldots (1)$$

where *R*driv and *C*driv is the driver resistance and capacitance, *Rw* and *Cw* are interconnects resistance and capacitance, "l" is the length of the wire, and *C*load is the load capacitance, it can be concluded that subthreshold interconnect delay is largely dependent on *R*driv and *Cw*.

In copper interconnects, repeater or buffer is basically implemented as CMOS inverter as shown in Fig. 1.for the design of CMOS inverter PMOS is assumed as 2.5 times of lmin. A CMOS inverter is used to drive interconnect load as shown in Fig. 1. The CMOS inverter is the simplest buffer or repeater in VLSI interconnects. Fig.1. shows a CMOS buffer driving a interconnect load and its equivalent symbolic representation. Fig.2. gives the equivalent RC and RLC lumped model representations of a long interconnect line. The short channel CMOS inverter delay becomes less to the input waveform slope and to the Vdd variation as compared to the conventional MOSFETs based on the square law model.

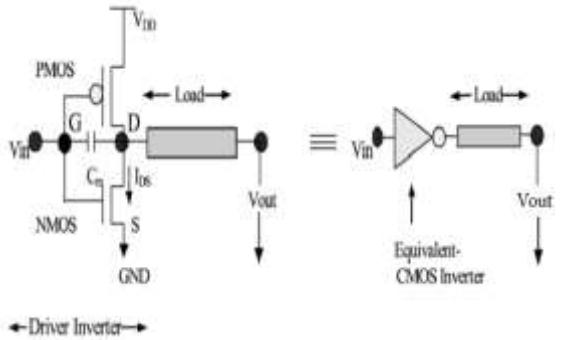

Figure 1.CMOS buffer driving an interconnect load.

The linear resistor capacitor delay method can be used empirically to calculate the delay in digital CMOS circuits. SPICE simulation is used here to get the analytical results. The current through both the transistors and gate to drain coupling capacitance are taken into account. Interconnect load can be represented by R, L and C parameters. Its RC/RLC lumped model is shown in fig. 3.

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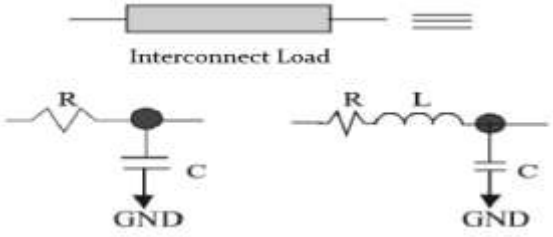

Figure 2. Interconnect load represented by RLC lumped model.

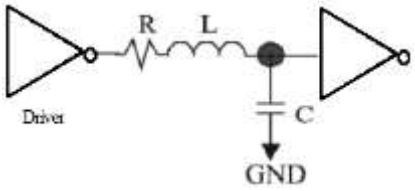

Figure 3.Driver interconnect load.

The physical geometries of interconnects determines the R, L and C parameters per unit length. The space between adjacent interconnects is same as interconnect width.

MOS CURRENT MODE LOGIC (MCML):

MOS current mode logic (MCML) is a popular logic style for high-speed circuits. This type of logic was first implemented in bipolar technology and extended for application with MOS transistors. This logic style is promising kind of in both reducing power consumption with the scaling of input voltage, for high Speed and providing an analog friendly environment. These properties make MCML topology as a robust technology. This requires the circuit to be biased in the subthreshold region. This circuit conducts a very low tail current with the production of huge output swing. It has numerous advantages over conventional CMOS. figure 4 shows MCML circuit. The pull-up load resistors are typically PMOS transistors. During the low-to-high transition, the PMOS pull-up network charges the output to VDD, unlike NMOS, which charges the output to VDD −Vth.

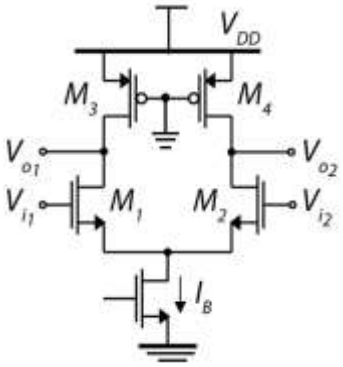

Figure 4. MOS Current mode logic (MCML) Inverter [3].

Operation of MCML:

The MCML cell consists of four main blocks, namely, the logic functional block, current source, power switch, and the load[3]. The logic function is implemented using a differential pair of NMOS transistors. Depending on the complexity of the function levels, the NMOS transistors need to be stacked one upon the other to implement the logic function. The current source will provide a constant tail current Iss. This current will be switched by the logic function to one of the output branch, which will eventually reach voltage level which corresponds to logic '0' due to the entire current flowing through the load resistor. The other output will stay at logic '1'. The operation is elaborated in the next section. The power switch is used to cut the current to the transistors during sleep mode, which will force both the outputs to logic '1', since there will be no current in the output branch.

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For a typical MCML circuit, the design parameters include the total power dissipation, circuit delay, voltage swing and voltage gain. These parameters can be controlled by the variables such as bias current, differential pull-down network transistor sizes, the current source transistor size and the current source bias voltage.

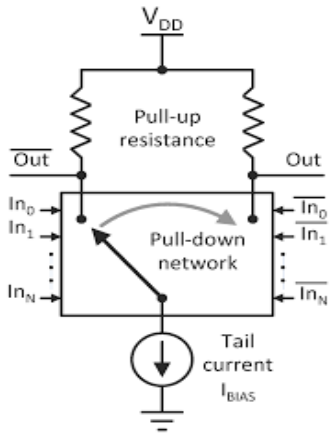

Figure 5.Operation of MOS Current mode logic.

The output voltage transfer characteristics of this inverter can be calculated once we know the equivalent resistance RD, so the differential voltage Vo is:

$$Vo = Vo1 - Vo2 = -R(iD1 - iD2) \quad \ldots (2)$$

CIRCUIT DESIGN

In order to get a fair analysis of the benefits of MCML over CMOS logic and Schmitt trigger as drivers, the design was carried out using minimum size transistors. The Circuits were operated at subthreshold voltage, The current source was implemented using a single transistor in order to have higher area efficiency. The load transistors were made as close to minimum size as possible as increasing their width will decrease their linearity and increase the capacitance which will slow down the circuit.

In order to make the MCML circuit operational in sub-threshold region, the transistors comprising the PDN were made to operate in sub-threshold region by scaling the gate voltages. The control voltages were scaled accordingly so as to keep current source transistor in saturation region and load transistors in linear/triode region.

Calculations of current and voltages for Fig.4 (MCML Inverter) are as follows:

VOH= VDD ... (3)

VOL= VDD – I * R ... (4)

Here VOH and VOL are maximum and minimum value of output voltages (Vout), R is the resistance offered by a PMOS (operating in linear region of operation)

On subtracting equation (3) and (4) we have:

VOH--VOL=I * R

ΔV= VOH--VOL=I * R ... (5)

Equation (5) shows the dependence of the output voltage swing on the two currents.

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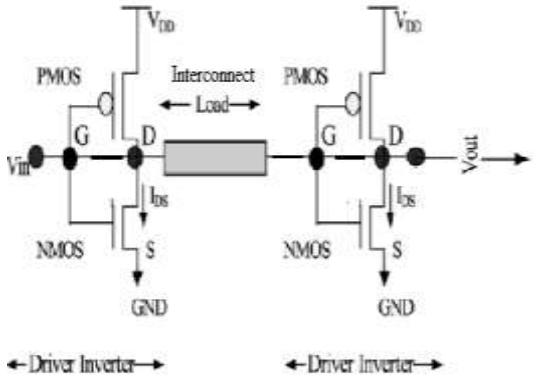

Figure 6.CMOS Driver Interconnect.

Fig 6.shows CMOS Driver interconnect, here CMOS drivers are used to drive the interconnects.

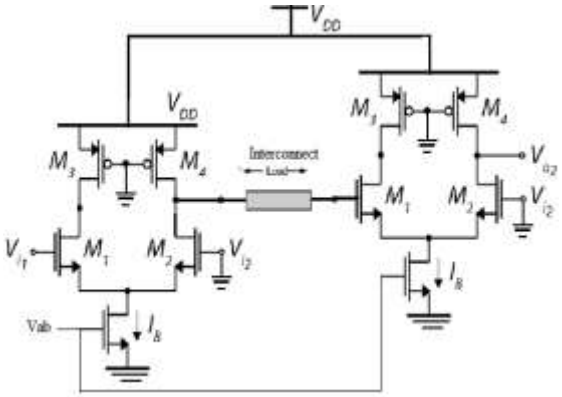

Figure 7. MCML Driver Interconnect.

Fig 7. Shows MCML driver interconnect which is a proposed circuit which helps to reduce the delay. The circuit is operated at 400Mv with width of NMOS is 1.5 times the minimum length, width of PMOS is 2.5 times the width of NMOS.

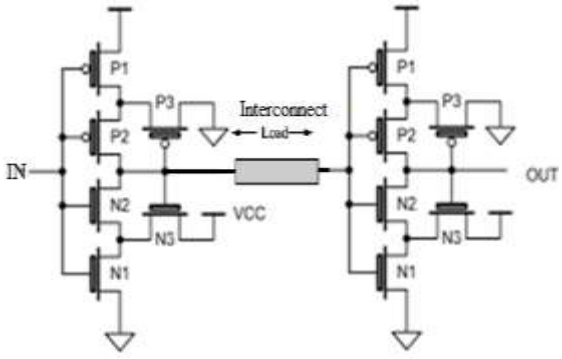

Figure 8. Schmitt trigger Driver Interconnect

Fig 8. Shows Schmitt trigger interconnect which is designed so as to compare its results with CMOS and MCML driver interconnects.

RESULTS AND DISCUSSION

All the simulations for Interconnects designed using Static CMOS, MCML and Schmitt trigger driver interconnect have been performed at supply voltage 400mV. It can be observed that when the gate voltage of transistor (current

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source implemented using transistor) in MCML is scaled, the delay also decreases which is contrary to that of static CMOS logic inverter.
This also leads to a decrease in PDP as the input voltage is scaled down contrary to CMOS logic. Also, in sub-threshold region, the static CMOS inverter shows a drastic increase in delay with decrease in supply voltage whereas in the case of MCML the average delay still decreases. At subthreshold region, the total delay of MCML inverter is much lesser than that of CMOS inverter driver interconnect. So, MCML topology finds application where high speed is our primary concern. MCML logic circuits operating in subthreshold region combines both low power and lower delay results in lower PDP contrary to CMOS logic circuits.
Various performance measures like delay, Power delay product (PDP) and Energy delay product (EDP) are compared for both MCML and CMOS logic circuits and their trade off is observed.

Table 1.Result analysis for MCML, CMOS and Schmitt trigger Interconnect driver

Parameters	Tpd	PDP	EDP
MCML	2.76E-11	7.01E-17	2.26E-27
CMOS	6.7E-09	1.01E-14	7.07E-23
Schmitt trigger	5.38E-09	6.64 E-16	3.57E-24

From the results we can see at 32nm technology node, MCML driver interconnect shows significant improvement in total delay, PDP and EDP performance as compared to CMOS driver interconnect & Schmitt trigger driver interconnect. Hence the speed of MCML driver interconnect is very as compared to other driver Interconnects.

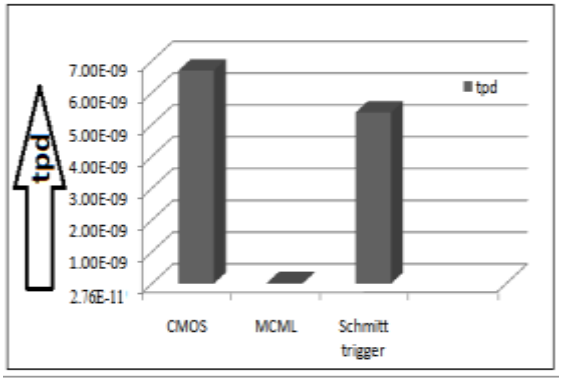

Figure 9.Tpd graph for CMOS,MCML and Schmitt trigger Driver Interconnect.

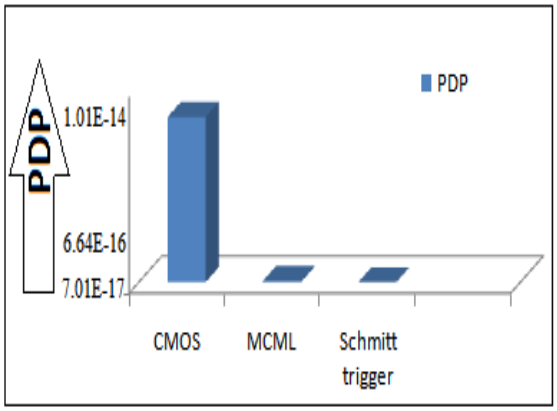

Figure 10.PDP graph for CMOS,MCML and Schmitt trigger Driver Interconnect.

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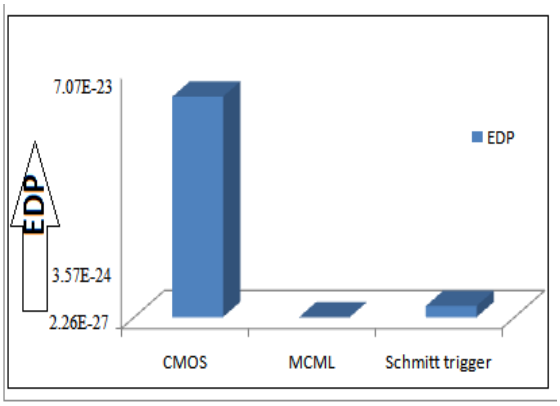

Figure 11.EDP graph for CMOS,MCML and Schmitt trigger Driver Interconnect.

CONCLUSION

In this paper, we describe the interconnects and designed the MCML (MOS Current mode logic) driver interconnect along with CMOS and Schmitt trigger driver interconnect in HSPICE. It has been investigated that delay in MCML is very less as compared to that of CMOS and Schmitt trigger driver interconnect .Under subthreshold region the total delay and PDP is less, which helps to operate the MCML Interconnect at high speed.

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